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TECHNOLOGY UTILIZATION

ELECTRONIC CIRCUITS AND SYSTEMS

A COMPILATION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Foreword

The National Aeronautics and Space Administration has established a Technology Utilization Program for the dissemination of information on technological developments which have potential utility outside the aerospace community. By encouraging multiple application of the results of its research and development, NASA earns for the public an increased return on the investment in aerospace research and development programs.

This document is one in a series intended to furnish such technological information. Divided into three sections, it describes a number of electronic circuits and systems. Section 1 contains descriptions of circuit components such as filters, converters, and integrators. Section 2 presents circuits designed for use with specific equipment or systems. The circuits in Section 3 were designed primarily for use with optical equipment or displays.

Additional technical information on the articles in this Compilation can be requested by circling the appropriate number on the Reader Service Card included in this Compilation.

The latest patent information available at the final preparation of this Compilation is presented on the page following the last article in the text. For those innovations on which NASA has decided not to apply for a patent, a Patent Statement is not included. Potential users of items described herein should consult the cognizant organization for updated patent information at that time.

We appreciate comment by readers and welcome hearing about the relevance and utility of the information in this Compilation.

Jeffrey T. Hamilton, *Director*
Technology Utilization Office
National Aeronautics and Space Administration

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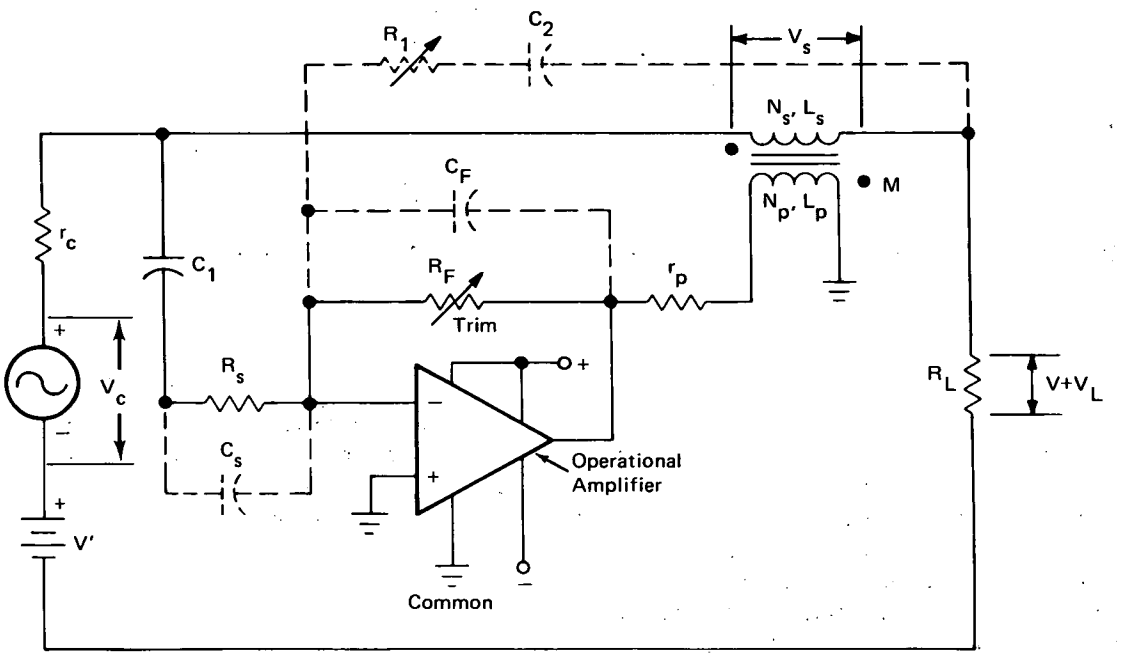
Contents

Section 1. Electronic Components and Circuits

ACTIVE RIPPLE FILTER



An active ripple filter has been developed to attenuate the residual ac components of a dc-rectified power supply. The filter circuit contains a wide-bandwidth low-distortion operational amplifier and a mutual inductor. The amplifier output is directly proportional to changes in the input voltage.

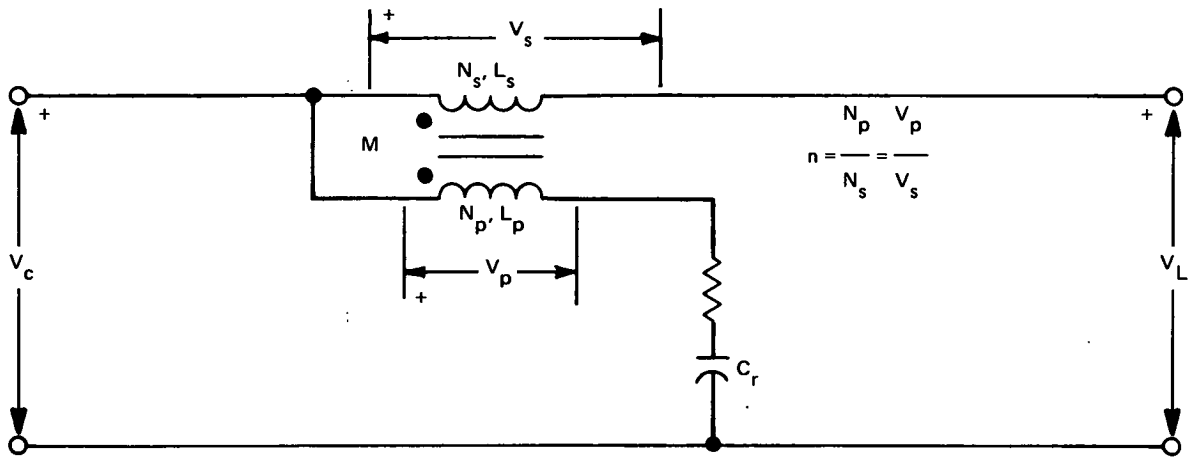
The circuit is shown in the figure. The dc input voltage is represented by a battery (V'), and the output is the voltage across the load, R_L. The input ripple voltage is V_c, and the output ripple voltage is V_L. Capacitor C_1 blocks the dc input and couples the ac input component to the amplifier with no change in phase or amplitude. The gain and phase shift of the amplifier and the turns ratio of the inductor are chosen so that $V_s \approx V_c$. Thus the output ripple, $V_L = V_c - V_s$, is very small. For the wide-bandwidth case, the feedback components, shown as dashed lines in the figure, can be added to further reduce V_c.

The circuit is very efficient because there are no dissipative elements in the main dc path. It accomplishes the same attenuation over a given bandwidth as an L-section filter, but uses only a few microfarads of capacitance. An L-section filter with the same inductance would require hundreds of microfarads to achieve the same results. Thus, this unit is smaller and more reliable.

Source: Sam Y. M. Feng, William A. Sander III, and Thomas G. Wilson of Duke University under contract to NASA Headquarters (HQN-10655)

Circle 1 on Reader Service Card.

PASSIVE RIPPLE FILTER



A ripple filter for dc-to-dc converters or for ac-to-dc power supplies has been developed. It is similar to the active ripple filter described in the preceding article, but it uses only passive nondissipative elements. The filter achieves considerable capacitance reduction in comparison to the conventional L-section filter used for the same purpose. Because of this capacitance reduction, more reliable types of capacitors with lower capacitance-to-volume ratios may be used, such as ceramic or mica, rather than the commonly-used tantalum units.

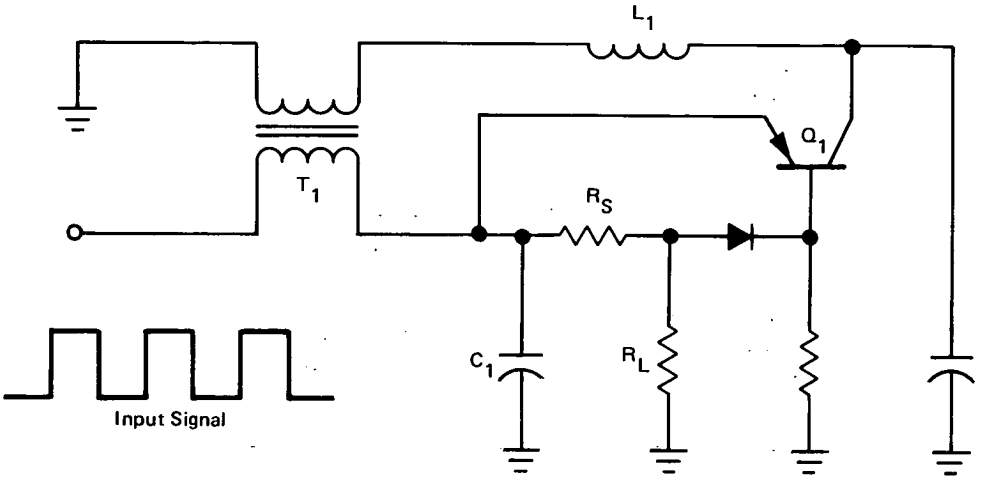
The ripple voltage, V_c, at the input to the filter is sensed and then regenerated on the secondary winding, N_s, of the mutual inductor, M (see figure). If the waveform of the induced voltage, V_s, across secondary winding N_s due to V_p is nearly equal to the ripple voltage (V_c) at the filter input, then the load ripple voltage ($V_L = V_c - V_s$) is very small.

A reduction in capacitance of 65% is realized easily with this filter compared to conventional filters. Two or more may be cascaded to provide a wider bandwidth and better attenuation.

Source: Sam Y. M. Feng, William A. Sander III, and Thomas G. Wilson of Duke University under contract to NASA Headquarters (HQN-10656)

Circle 2 on Reader Service Card.

LOW-PASS INDUCTIVE-INPUT FILTER



To effectively filter complex signals with inductive-input impedance characteristics, low-permeability core materials have been used in the past. These required many coil turns to achieve a given filter performance and efficiency was lost. Alternatively, high-permeability material with a large core was used, with a size penalty. In addition, the use of high-permeability materials where dc currents had to be transmitted always resulted in a low effective permeability.

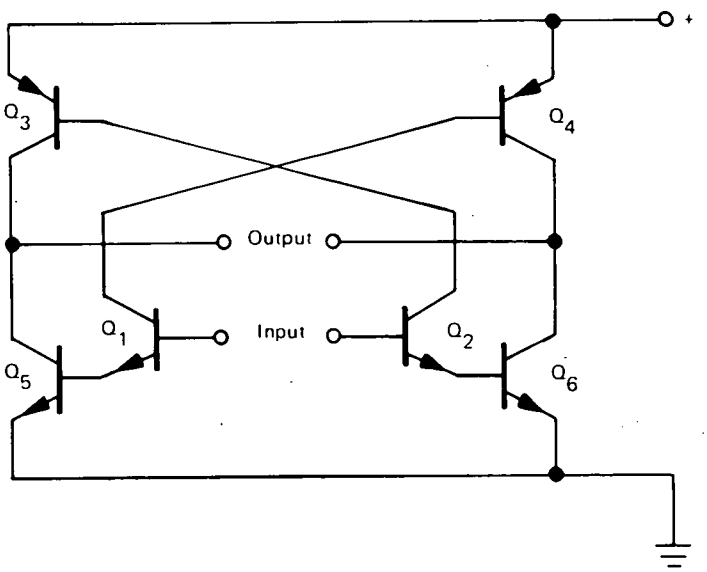
A filter has been designed that offers the same performance at high dc levels as that obtainable at zero dc, with no size penalty. The core of the filter inductor is prevented electronically from saturating and degrading the filter performance. Thus, the filter works well, independently of the dc level, and access is always available to the high permeability of the core.

The circuit is shown in the figure. The primary of T_1 and C_1 are the basic filter elements. The average current through the T_1 primary will saturate its high-permeability core, thus degrading the filter attenuation characteristics. This is precluded by the reset current in the T_1 secondary which is supplied by a transistor current source (Q_1). As the average primary current varies, the reset current is varied, due to the voltage developed at the sensing resistor (R_S) and is applied to the emitter and base of Q_1.

Source: R. T. Buchholz of
Lockheed Electronics Company
under contract to
Johnson Space Center
(MSC-11954)

No further documentation is available.

BRIDGE-OUTPUT CIRCUIT



Complementary bridge circuits are widely used. However, there are several difficulties inherent in most of them. It is difficult to drive all four elements of a bridge, to control the maximum current, and to prevent both elements on one side of a bridge from conducting simultaneously and shorting the power supply.

A dc-coupled circuit that has been devised to overcome these problems is also suitable for construction as an integrated circuit. Standby current in the circuit is negligible, and crossover transients can be suppressed. If the transistors are driven to cutoff, the efficiency will be high, because most of the voltage drop will appear across the load.

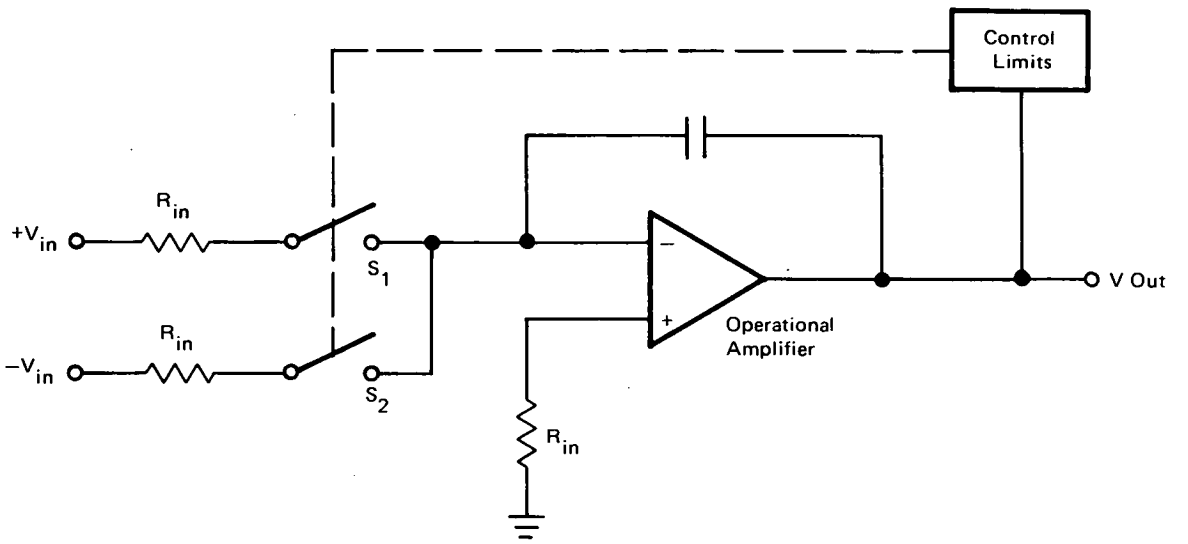
The basic arrangement of the circuit is shown in the figure. Current flows through Q_1 and turns on Q_4 and Q_5. At the same time, current flowing through Q_2 turns on the other side of the bridge. Thus Q_1 and Q_2 can be driven out of phase for push-pull operation.

The basic circuit shown in the figure may be modified to improve linearity and to handle large current.

Source: W. N. Jones of
Westinghouse Electric Corp.
under contract to
Johnson Space Center
(MSC-13442)

Circle 3 on Reader Service Card.

SELF-COMPENSATING LOW-DRIFT INTEGRATOR



A self-compensating low-drift integrator has been developed. Improvements have been obtained in reset error, output range, and drift.

When the integrator reaches its output limit, control circuits quickly reverse the states of S_1 and S_2 (see figure). Thus reset error, caused by the time required to discharge fully the feedback capacitor C in a conventional circuit, is eliminated.

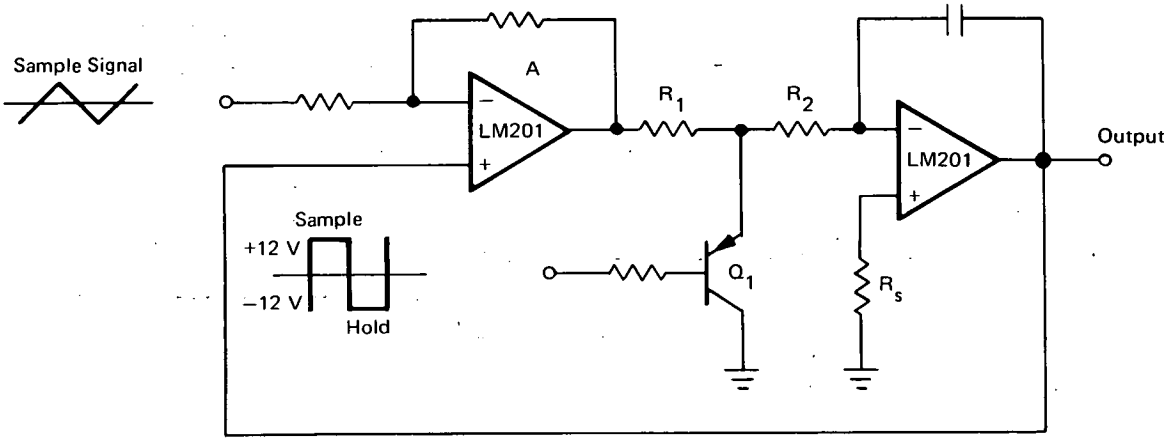
The output of a conventional integrator can be no higher than the amplifier supply voltage, V_S. Conventional reset is to zero volts, and the range is zero to V_S. This new circuit lengthens the cycle time by a factor of four, or increases the effective range to 4 V_S.

The usual causes of drift are amplifier offset voltage and offset current, which cause the inverting input of the amplifier to be at a nonzero potential (acting like a false input signal). Switching the input polarity effectively cancels out these errors by averaging.

Source: Clement A. Berard, Jr., and
James L. Douglas of
RCA Corporation
under contract to
Goddard Space Flight Center
(GSC-11235)

Circle 4 on Reader Service Card.

SAMPLE-AND-HOLD CIRCUIT



Sample-and-hold circuits require complex circuitry to obtain accurate results. A new circuit with a feedback loop performs this operation on both positive and negative signals and is not limited only to peak values. This principle leads to a simplified circuit configuration.

A signal is sampled when the voltage at the base of Q_1 (see figure) is changed from +V to −V, which is controlled by an external source. The output voltage then remains at the precise level of the input at the time sampling occurred; the output circuit has a very low impedance. During sampling, the input signal is amplified by A. The loop serves to null the error between input and integrator output, when the input to the integrator is zero. The feedback loop allows the conventional complex combination of a peak detector and high-input-impedance amplifier to be replaced with this simple circuitry that has the same accuracy.

Source: N. C. Lerche and A. F. Errington of
Lockheed Electronics Company
under contract to
Johnson Space Center
(MSC-11957)

Circle 5 on Reader Service Card.

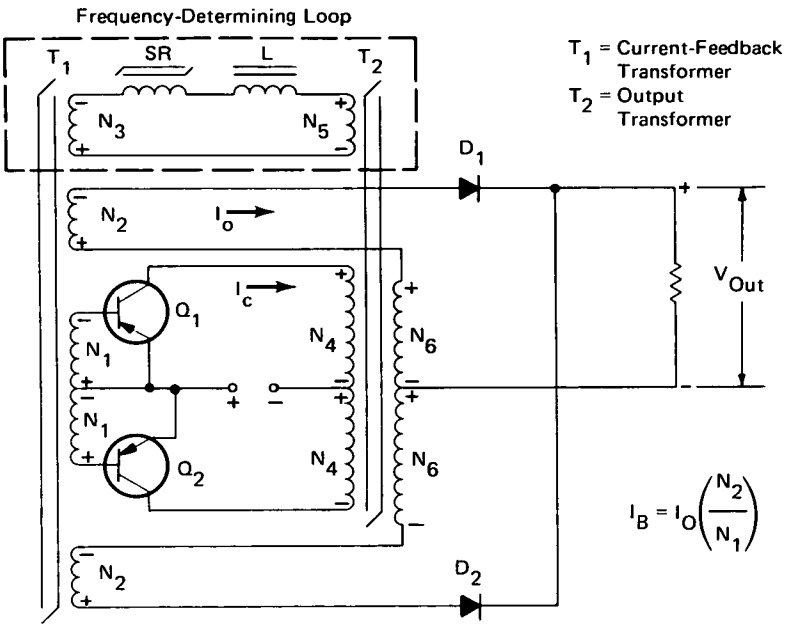
BIDIRECTIONAL SAMPLE-AND-HOLD CIRCUIT

A sample-and-hold circuit has been developed that is capable of charging storage capacitors for signals with both positive and negative slopes. Previous circuits operated on only positive-slope inputs. This new circuit offers superior control of junction offsets through the use of a monolithic dual transistor as a diode. Other advantages of this circuit are low power dissipation, high input impedance, and large-output time constant. Complementary circuitry allows one branch or the other to operate, depending upon the polarity of the input signal relative to the previously stored voltage.

Source: Roy H. Stehle of
Stanford Research Institute
under contract to
Goddard Space Flight Center
(GSC-11081)

Circle 6 on Reader Service Card.

DC-TO-AC-TO-DC CONVERTER



Inverter with means for base-current shaping for sweeping charge carriers from base region. (Polarities are shown for half cycle when Q_1 and D_1 are conducting; for other half cycle, polarities reverse, and Q_2 and D_2 conduct.)

Previously, a dc-to-ac-to-dc converter utilized a dc-to-ac inverter, including a pair of switching transistors driven in push-pull. Output electrodes of the transistors were connected to the primary windings of a first transformer, the secondary windings of which were connected through a frequency-determining network to a second transformer. The secondary windings of the second transformer drove the base circuitry for the switching transistors. Voltages derived in a secondary winding of the first, or output, transformer were rectified to dc with a full-wave rectifier, including a pair of diodes.

While this circuit functioned satisfactorily, it was not efficient enough for some purposes. For low-dc-load voltages, the voltage drop across the rectifiers was a significant percentage of the voltage developed across the load. Further, the I^2R power dissipated in diode was appreciable, requiring a heat sink in some instances.

These problems have been reduced substantially by employing a synchronous rectifier (see figure) including a pair of transistors having their bases driven with the same waveform as the transistors of the dc-to-ac inverter. The synchronous rectifier transistors are driven quickly from a conducting to a nonconducting state, and vice versa, in a mono-overlapping manner; this is due to the shape of the driving waveform.

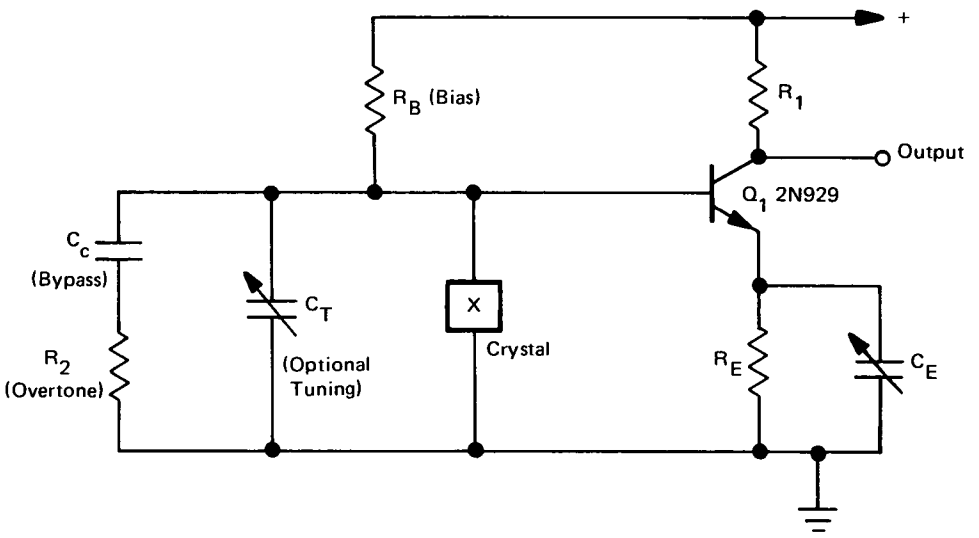
The bases of these transistors are connected to separate secondary windings, which are coupled to the base drive for the switching transistors of the inverter. Energy is coupled to the bases in a very efficient, almost lossless, manner, independent of the load requirements.

This new circuit provides an improved dc-to-ac-to-dc converter that is highly efficient, substantially precludes short circuits, has good regulation, and has a relatively-low ripple factor.

Source: Edward R. Pasciutti
Goddard Space Flight Center
(GSC-11126)

Circle 7 on Reader Service Card.

INTEGRATED-CIRCUIT CRYSTAL OSCILLATOR



Design techniques for conventional crystal oscillators are well established. However, components such as fixed or variable inductors and variable capacitors are virtually nonexistent in integrated-circuit form. A novel design for a crystal oscillator has been developed to circumvent this problem. The design permits a minimum number of components and may be fabricated as an integrated circuit.

In this circuit (see figure), a transistor is connected as an emitter follower. The premise upon which operation is based is that the beta of a transistor in the region of the transitional frequency F_T may be considered as

$$\beta = -J\frac{F_T}{F}$$

where F_T is the frequency at which beta is unity, and F is a frequency in the general region, but lower than F_T. The effective capacitance at the input of Q_1 then exhibits a negative resistance which is used to sustain oscillation. The crystal operates between the series resonant point and the parallel resonant point, or in the inductive mode.

A fifth overtone crystal can be used; and, by selecting resistance values, fundamental, third, or fifth overtones are available. The oscillator performs over a wide range of supply voltages.

Source: L. Kleinberg
Goddard Space Flight Center
(GSC-10137)

No further documentation is available.

POWER INVERTER WITH SINUSOIDAL OUTPUT

Present electrical power inverters (dc to ac converters) can be divided into two classes: (1) inverters with a square-wave output followed by low-pass filters to produce sinusoidal power and (2) inverters with resonant circuits directly in series with the load or in parallel with the load.

A new inverter has been developed in which the transistors are operated more efficiently and safely than in square-wave inverters, because switching occurs when the sine-wave collector current is zero. Additional efficiency is obtained because harmonic currents are almost completely inhibited in the inverter, and only rectified sine-wave currents are drawn from the input bus. The small harmonic content results in unusually-low electromagnetic interference.

This circuit is an improvement over those which operate directly in series or in parallel with the load, because the resonant circuit is isolated from the load by the output transformer. The resonant circuit can be designed so that the resonant frequency is independent of the load. This is of particular value when the load impedance affects the operating frequency at both high- and low-output voltages.

Source: E. J. Miller of
Martin Marietta Corporation
under contract to
Marshall Space Flight Center
(MFS-21967)

Circle 8 on Reader Service Card.

MULTIFUNCTION LOGIC-GATE CIRCUITS

A logic gate has been devised with two or more outputs that produce several different logic functions of the same input signal. Previously, when more than one function of the input signal was to be obtained, two or more logic gates were necessary.

The logic gate is an N-input gate having two outputs that concurrently produce a function at one output and produce the complement of its dual or another desired function at the other output. The signal is applied to the base of one transistor of a pair, while the base of the other transistor receives a reference signal. A pair of these transistors is needed for each input signal. By choosing the load resistances for these transistors, output functions are implemented.

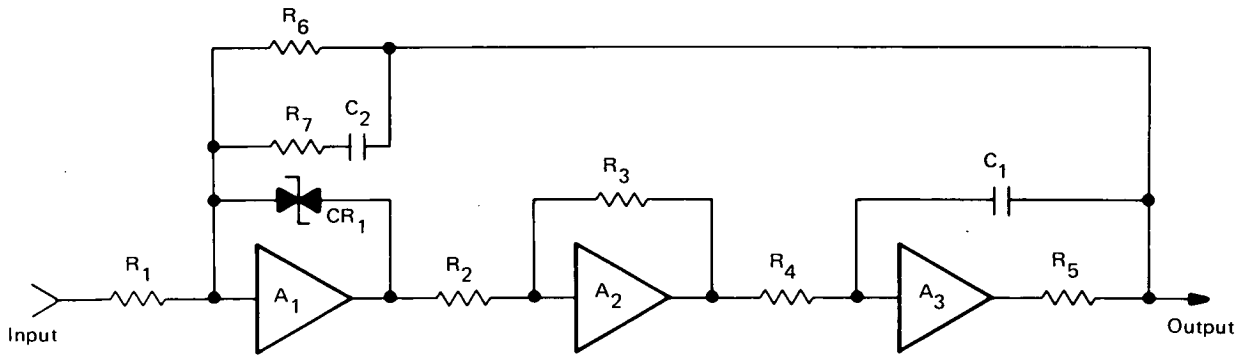
This circuit lends itself to construction as an integrated circuit, or since precision resistances are required, as a hybrid circuit.

The following documentation may be obtained from:
National Technical Information Service
Springfield, Virginia 22151
Single document price $6.00
(or microfiche $2.25

Reference: NASA-CR-1668 (N70-41983) "Threshold Logic Implementation of a Modular Computer System"

Source: Daniel Hampel of
RCA Corporation
NASA Headquarters
(HQN-10702)

OPERATIONAL SLOPE-LIMITING CIRCUIT



A new circuit limits the slope of an arbitrary waveform in order to avoid exceeding the rate limit of a subsequent amplifier. The circuit consists of an amplifier, an inverter, and an integrator; the integrator provides the delay needed to develop the output waveform. DC coupling is used to preserve the original dc offset.

The circuit is shown in the diagram; the output of the first of three general-purpose operational amplifiers is bridged to its input by a double-anode zener or two closely-matched back-to-back zeners (CR_1) with breakdown voltages within the excursion capability of the amplifier (say, 8 volts). The amplification of the second amplifier (an inverter) is set approximately at unity by resistors of the order of 10 kilohms (±5%). The input resistor to the last amplifier is set at a few kilohms to 100 kilohms or more, and the integrating capacitor can be from 100 pf or less to 1 mfd or more in order to set the slope limit. For adjustable slope operation, the input resistor to the last stage may be variable and the capacitor value is altered by switching. The output resistor in the last stage is optional but, if used, it determines the circuit output impedance, and permits use of large capacitances which otherwise must be limited to about 0.05 mfd by the choice of the operational amplifier. The main feedback resistor, R_6, and the input resistor, R_1, determine the overall gain of the circuit; generally, they will be a closely-matched pair (say, 10 kilohms each). The series resistor-capacitor combination, R_7 and C_2, across R_6 compensates the loop gain which, for a small signal, is the product of the gains of the first and third amplifiers (typically about 200 dB); the RC combination also stabilizes the gain. The optimum value of the RC combination is determined empirically, and will be governed by the characteristics of the operational amplifiers, but if the integrating capacitor, C_1, is switched, then the RC compensating combination must also be switched.

When the input signal changes rapidly, the output is prevented from following it by the delay in the integrator; consequently, a large error exists in the loop and the output of the first amplifier rises until it is clamped by CR_1. A constant voltage is applied to the inverter, causing the integrator to slew at a uniform rate until the output very nearly equals the input.

When the change of input signal is sufficiently slow to allow the integrator to keep up with it, the circuit operates linearly, exactly reproducing the input waveform. (Note that the output signal is inverted in polarity with respect to the input.)

Source: Alexander Engel of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-11773)

Circle 9 on Reader Service Card.

Section 2. Specialized Circuits

ALL-DIGITAL DEFLECTION CIRCUIT

The thrust of an ion engine may be deflected by a small lateral translation of the accelerator electrode with respect to the screen electrode; the two electrodes form a pair of parallel planes separated by a few millimeters.

One method of deflection is to utilize the differential thermal expansion of support legs, which consist of eight coaxial electric-heater elements arranged to operate in pairs. The system is designed for a maximum deflection of $\pm 7^{\circ}$, in which range the deflection is proportional to heater power.

The digital control system provides four-bit resolution (zero deflection and fifteen steps in each direction). Previous systems converted digital command signals to analog signals. The new system eliminates drift problems arising from the digital-to-analog converter.

The circuit counts the cycles of the 10-kHz system power and treats them as separate periods of 256 cycles each. It then switches a selected fraction of the cycles to the proper heater pair, through a stepdown transformer. This is accomplished by comparing the count in a four-bit command register with the count in a continuously-running four-bit counter counting the 10-kHz cycles. When the 10-kHz counter fills and resets to zero, the power-switch transistor is turned on. When the comparator senses that the 10-kHz counter and the command register contain the same count, the transistor is turned off.

There is a separate switch transistor for each deflection polarity (X^{+1} and X^{-1}), and a flip-flop ensures a polarity change every 16 cycles. An identical circuit is used for the Y axis.

Source: Robert M. Worlock and
Gale D. Gant of
Xerox Corporation
under contract to
Goddard Space Flight Center
(GSC-11343)

Circle 10 on Reader Service Card.

ARC-DIPPER CIRCUIT

The problem of plasma extrusion in ion engines is frequently encountered. This forcing out of plasma in the discharge chamber, between the screen and the accelerator electrodes, is caused when high voltages on the electrodes are removed, as happens briefly during a spark discharge.

The problems resulting from plasma extrusion have been overcome by the use of an arc dipper, which reduces the voltage supplied to the discharge chamber, in response to overloading the high-voltage supplies. In this way, when a spark occurs, the strength of the electrostatic field in the discharge chamber is reduced momentarily, with an attendant decrease in the amount of plasma extruded between the electrodes to minimal levels.

The arc-dipper circuit is comprised of an operational amplifier, with an input connected to the high-voltage overload circuits, for controlling switching of a control-transistor supply circuit. By turning off the control transistor, the arc in the discharge chamber is dipped. A feedback loop ensures that the discharge voltage returns to the nominal level at a gradual rate, 20 volts per second or less. A monostable multivibrator, responsive to plasma anode-current overloads, is also connected to the same transistor switching circuit.

Source: R. M. Worlock and G. Gant of
Xerox Corporation
under contract to
Goddard Space Flight Center
(GSC-11344)

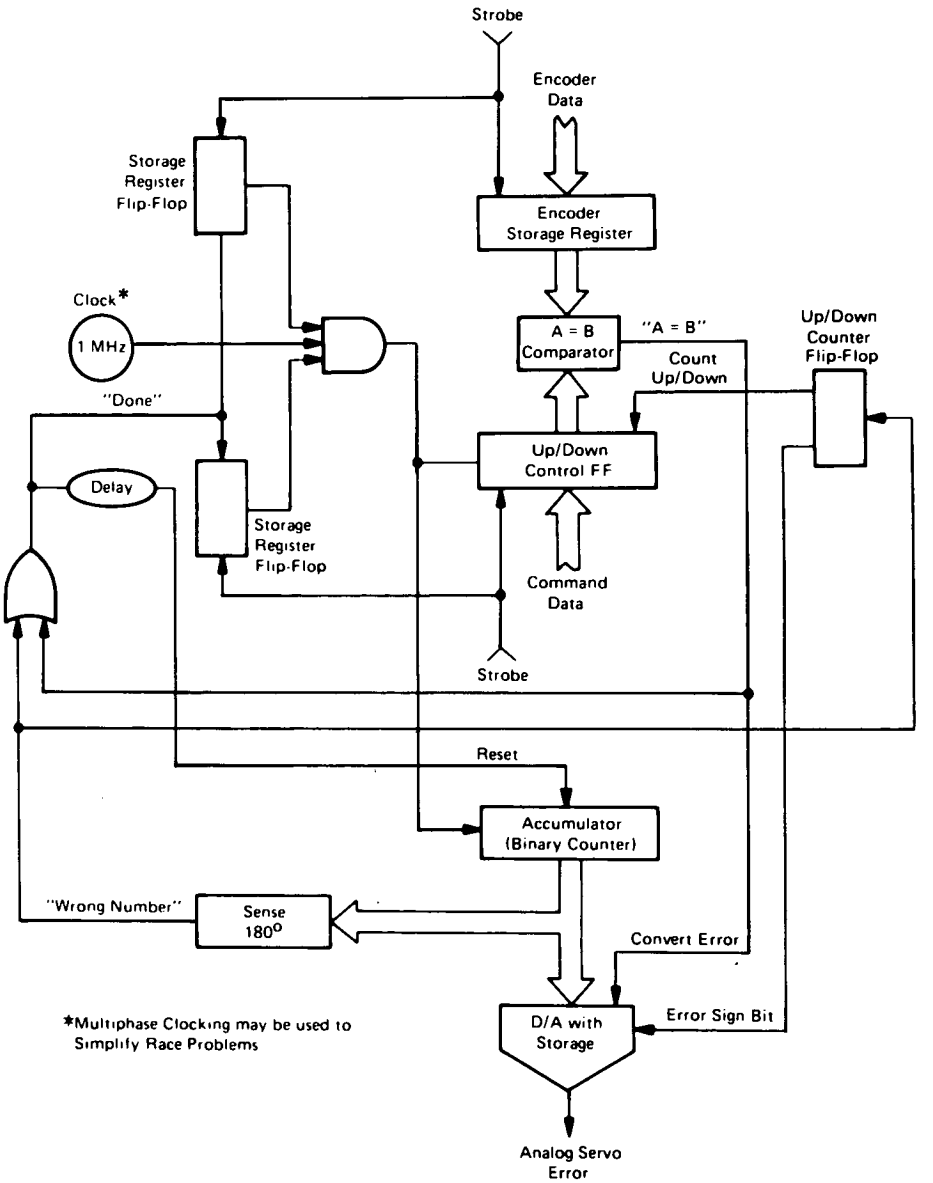
Circle 11 on Reader Service Card.

DIGITAL SERVO CONTROLLER BEHAVES LIKE SYNCHRO

The rotation of shafts supporting directional antennas requires a precise control for accurate angular positioning. The synchro-demodulator servo system has been a popular element for this type of control because of its unique inherent ability to "compute" the shortest distance between desired and actual positions, and because it can resolve unambiguously and monotonically all portions of its normal 360° travel. The synchro is generally very rugged, but has limited accuracy (±0.1°). In the world of digits (computer control, etc.) the synchro is unwieldy and interfacing is expensive.

It is generally more accurate and simpler to interface with a digital encoder used as a shaft angle transducer. The encoder has been used for years to measure accurately the positional parameters of controlled devices with very high accuracy and reliability. A digital control system has been designed using digital shaft angle encoders.

The figure depicts a digital control system which provides error responses similar to synchros. The example is shown for BCD (binary coding), however, any common coding scheme can be similarly employed. The



Digital Servo Controller

control system computes the correct error magnitude and direction using a "cut and try" routine, based on the fact that the correct error can never be greater than 180° and the incorrect error will always be greater than 180°.

A shaft encoder signals the present position of the controlled device. A parallel BCD word commands the desired position for the controlled device. By means of suitable clocks, both the encoder word and the desired word are strobed into two registers, generating a "loaded" signal. The "loaded" command initiates control action which allows the clock to increment or decrement (depending on mode of direction flip-flop, FF) the up/down counter (assumed for this example to be loaded with the desired position). Simultaneously, the previously cleared accumulator is also incremented, count for count with the up/down counter.

When the digital value of the up/down counter matches the previously stored encoder value, or when the accumulator count exceeds a value of 180°, the incrementing process is terminated, and one of two following operations is performed. If the accumulator exceeds 180°, all counters are reset, the cycle is terminated, and no new error data is transferred from the error digital to analog (D/A) converter. Additionally, the direction flip-flop for the up/down counter is toggled (the controller made the "wrong" assumption with regard to the error magnitude and direction, and upon doing so ignored the generated error command but "corrected" itself for the next try). If, on the other hand, the register comparator signaled the end of the cycle, the controller "knows" that to be a correct solution and the resulting accumulator count is transferred to the error D/A converter.

Source: Frank Byrne
Kennedy Space Center
(KSC-10769)

Circle 12 on Reader Service Card.

HYBRID ELECTRONIC COMMUTATOR

Electronic commutation of dc motors is normally provided by discrete components. This is disadvantageous because the commutator should be within the motor shell and discrete components are large.

Hybrid circuits have been designed containing a complete motor commutator without sensors. They are capable of providing up to 0.5 ampere at 28 volts of three-phase full-wave power directly to the motor armature. Solid-state sensors, acting as switches, apply power to the motor windings in the correct phase sequence. The circuits contain their own logic to minimize the number of sensors, while assuring zero overlap and preventing switchthrough even if all sensors are accidently illuminated simultaneously. Standard 50-percent on 50-percent off encoder intervals provide the correct inputs. Access to the emitters of all output transistors is provided so that an order-of-magnitude higher power can be obtained, simply by connecting additional external devices in a Darlington arrangement.

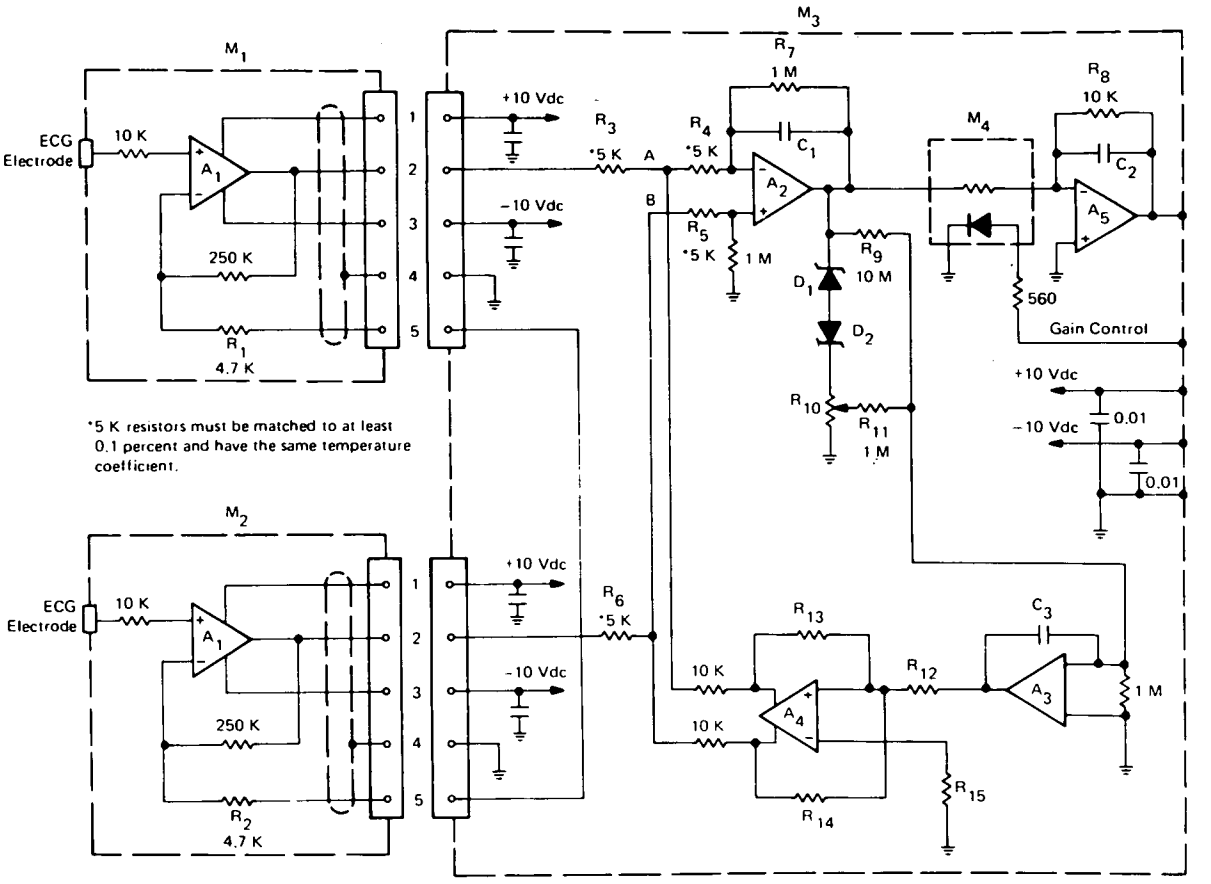
The system is contained in a hermetically sealed package offering smaller size, greater reliability and testability, lower cost, and, generally, a more practical form of electronic circuitry.

The fact that commutation circuits have only one of several channels operative at a given time makes it advantageous to construct them on a common substrate. Uniform temperatures and thus better performance are more easily obtained. The total peak load is only one-third of the individual peak load, since only one-third of the switches are on at a given time. This allows a total heat-sink area only one-third that required for discrete components.

Source: Philip A. Studer and
Cornelis deKramer
Goddard Space Flight Center
(GSC-10815)

Circle 13 on Reader Service Card.

ELECTROCARDIOGRAPH SIGNAL CONDITIONER



Conventional electrocardiograph (ECG) amplifiers are ac-coupled and have a low-frequency cutoff (0.01 to 0.05 Hz). The time required to recover from a momentary load is typically greater than ten seconds. A new signal conditioner shortens this time, while maintaining the low-frequency cutoff.

Recovery time is inversely proportional to the cutoff frequency. However, the addition of a recovery-control circuit cancels the offset drift and any signal below the cutoff frequency. This circuit provides a fast return to zero for momentary overloads that may range from dc to an upper-frequency cutoff.

The circuit is shown in the figure. Modules M_1 and M_2 (primarily existing technology) amplify the ECG signal and provide part of the common mode rejection. The output of M_3 is applied to a variable-resistance module (not shown) containing a photocell and a light emitting diode (LED). The variable-resistance module and amplifier A_5 form a variable-gain element that allows the gain of the ECG signal conditioner to be set.

Amplifiers A_3 and A_4 constitute the baseline stabilization control circuit and are a key part of the conditioner. The signal from A_2 is coupled to A_3 by R_9 and by diodes D_1 and D_2 or by R_{10} and R_{11} depending on the signal level.

When D_1 and D_2 are not conducting, components R_9, C_3, and A_3 form the low-pass filter for the required low-frequency cutoff.

In the linear range of the signal conditioner, A_3 provides a control voltage to A_4 that reacts to drift in A_2 and to changes in signal levels below the cutoff frequency. A_4 converts the single-ended output of A_3 to a differential output and applies the resultant signal to the input of A_2, thereby closing the loop.

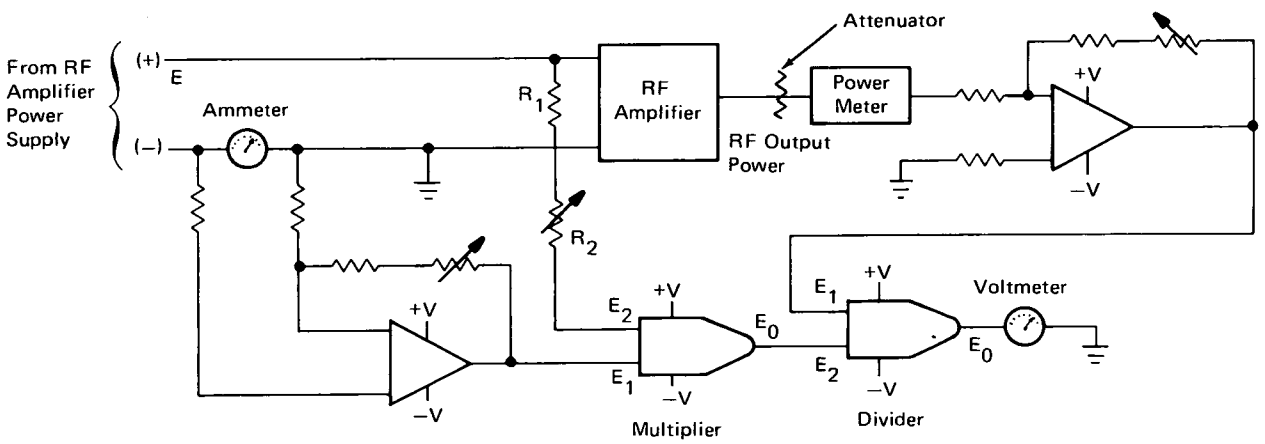
The signal applied to the input of A_2 opposes the changes that produce an output from A_2 below the low cutoff frequency, and tends to maintain the voltage input level of A_2 at ground potential plus or minus any offset in A_2. During momentary overloads caused by muscular activity of the subject or switching transients,

diodes D_1 and D_2 conduct and apply a much larger signal to A_3 through R_{11} than normally through R_9. This has the effect of decreasing the A_3 time constant and applying a large correction voltage to A_3.

Source: J. D. Evans of
The Boeing Company
under contract to
Johnson Space Center
(MSC-14033, 14034)

No further documentation is available.

METER CIRCUIT FOR TUNING RF AMPLIFIERS



A metering circuit has been developed to eliminate the many tedious calculations required when signal, bias, and power inputs are varied during tune-up of an RF amplifier for optimum efficiency. The circuit computes and indicates the efficiency of the RF amplifier as the inputs and other parameters are varied.

The metering circuit, shown in the diagram, includes a precision ammeter which indicates the dc current flowing from the power supply to the RF amplifier. The voltage drop across the internal resistance of the ammeter is amplified by an operational amplifier and applied to one of the inputs of a multiplier. The other input to the multiplier is obtained through two resistors from the positive terminal of the power supply. The multiplier output is thus proportional to the denominator of the efficiency equation, $\eta_c(\%) = P_{rf}/(I \times E)$.

The power output of the RF amplifier is fed to a power meter to provide a visible indication of the amplifier output. The power meter simultaneously generates a voltage that is proportional to the scale indication (within a range of 0 to −1 volt); the output voltage is amplified by an operational amplifier and applied to one of the inputs of a divider; the output of the multiplier is applied to the other input of the divider. The divider output voltage is thus the amplifier power output divided by the I x E power input to the amplifier and is representative of the efficiency of the RF amplifier for a given dc power and signal output. The conditions for optimum operation of an RF amplifier can be obtained more quickly with the aid of the meter circuit than when separate current, voltage, and power values must be obtained from meter readings and then used to compute overall efficiency by manual computations.

Source: James E. Longthorne of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-11865)

Circle 14 on Reader Service Card.

SIGNAL CONDITIONER TEST SET

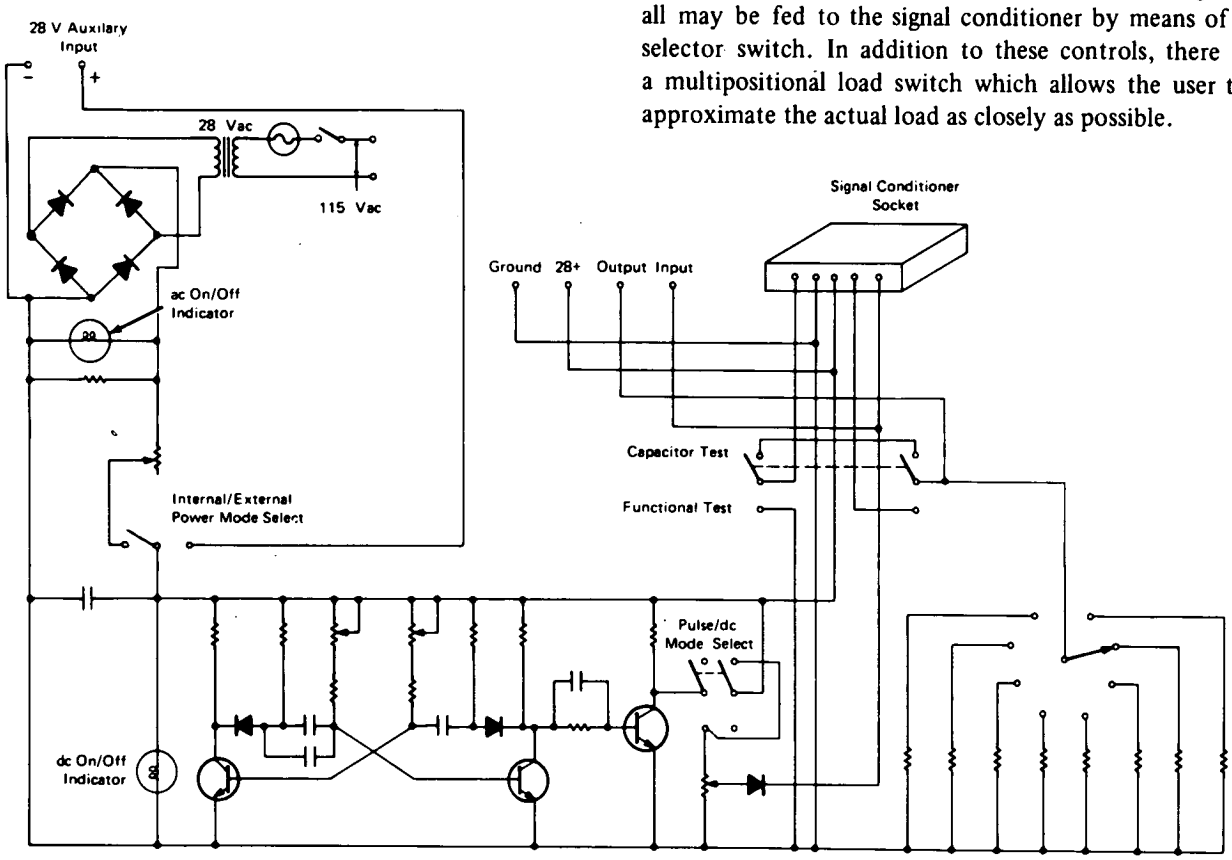
To check signal conditioners it is often necessary to remove them from the overall system; in some cases, they must be shipped to a laboratory for testing and study.

A compact, light-weight, solid-state test set can be used to check signal conditioning modules while they are installed in the system.

The test set, which operates from 115 Vac or 28 Vdc, indicates whether the signal conditioner is performing according to specification. In the case of the specific conditioner for which the set was designed, it indicates the condition of a specific capacitor that is subject to malfunction.

"on" voltage of one volt. Any intermediate voltage is also possible. The output consists of a variable amplitude waveform with logic levels compatible with standard conditioning equipment. Several known loads are available through a multiposition switch on the set. The oscillator output goes to a driver stage which feeds the signal conditioner under test.

There are several other controls and adjustments. A selector switch determines ac or dc power; although in either case 28 Vdc is available at external jacks. One fine control adjusts the period of oscillation, another the duty cycle, and another adjusts the amplitude of the waveform as seen by the signal conditioner. The oscillator signal, a straight dc voltage, or no voltage at all may be fed to the signal conditioner by means of a selector switch. In addition to these controls, there is a multipositional load switch which allows the user to approximate the actual load as closely as possible.



Test Set Schematic

A schematic of the test set is shown in the illustration. The set consists of an astable multivibrator with a 13.33% duty cycle which approximates the signal input to the conditioners in the system. The multivibrator oscillator has an "off" voltage of about 27 volts and an

Although this test set was designed for a specific conditioner, it may be used with any conditioner with compatible logic levels by means of external jacks provided to feed an input signal, a load for the conditioners, and power if needed. In any case, before using

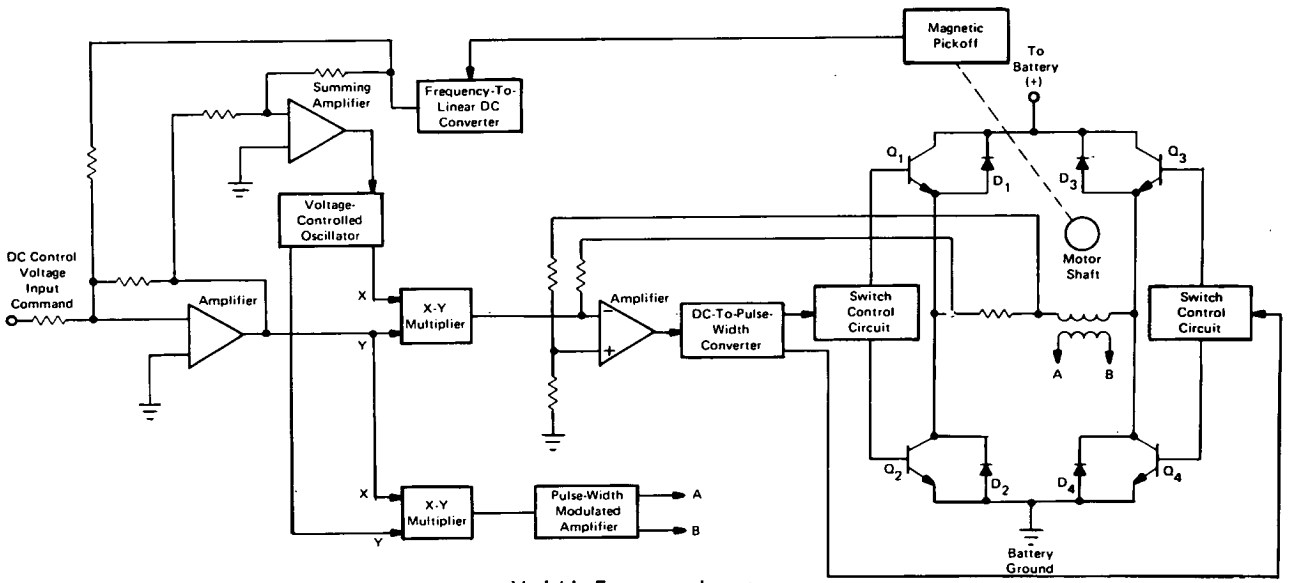
the set it may be necessary to adjust the frequency or duty cycle if they are critical.

Another feature of this test set is that it may be used to cycle the ground computer, if it is suspected of malfunctioning, rather than to use the signal conditioners. In this case, it may bypass the signal conditioner and provide a direct signal for the computer. Alternately, the test set feeds signals to the conditioners and from there to the ground computer.

Source: Walter H. Houck and Jon D. Stigberg
Kennedy Space Center
(KSC-10750)

Circle 15 on Reader Service Card.

VARIABLE-FREQUENCY INVERTER CONTROLS TORQUE, SPEED, AND BRAKING IN AC INDUCTION MOTORS



Variable-Frequency Inverter

A new variable-frequency dc to ac inverter provides optimum frequency and voltage to an ac induction motor, in response to different motor-load and speed requirements. The inverter varies the slip frequency of the motor in proportion to the required torque. In addition, the inverter protects the motor from high current surges, controls the negative slip to apply braking, and returns the energy stored in the momentum of the load to the dc power source.

As shown in the inverter block diagram, speed is set by a speed input command (dc) voltage level. Feedback voltage, generated by the frequency-to-linear dc converter, is combined with the command voltage in the summing amplifier and is applied to the voltage-controlled oscillator. A magnetic pickoff is used as a frequency sensor in the speed feedback loop. The oscillator output is multiplied by the control voltage to produce a sinusoid with an amplitude proportional to the control voltage. The sinusoid is converted to a pulse train, with variable pulse width, to feed the motor winding drivers.

The four drive transistors, Q_1 through Q_4, operate in pairs to alternate current flow through the motor winding. Q_1 and Q_4 are one pair, Q_2 and Q_3 are the other. Diodes D_1 through D_4 allow charge current flow back into the battery during braking. In this mode, the peak winding voltage (ac) exceeds the battery voltage, allowing the diodes to act as a bridge rectifier and conduct in pairs.

Source: F. J. Nola
Marshall Space Flight Center
(MFS-22088)

Circle 16 on Reader Service Card.

THREE-LEAD WHEATSTONE BRIDGE SYSTEM FOR REMOTE USE OF HOT-WIRE ANEMOMETER

The use of hot-wire anemometers in flow measurements usually depends upon the length of the cables connecting the wire, i.e., from the sensor to the bridge. The wire is an arm of the Wheatstone bridge of the anemometer. The length of the connecting leads and, hence, their resistance affect the bridge balance. Most of the available hot-wire anemometer systems are designed for specific lead lengths. Commonly, coaxial cable or four-lead connections are used. In order to measure the wire resistance and to balance the bridge under both cold and hot conditions, it is necessary to account for the resistance of the cables. The accepted length of the leads is limited to about 6 to 9 m (20 to 30 ft). The cable length constraint is a shortcoming when longer leads are needed, particularly, in the remote use of hot-wire anemometers.

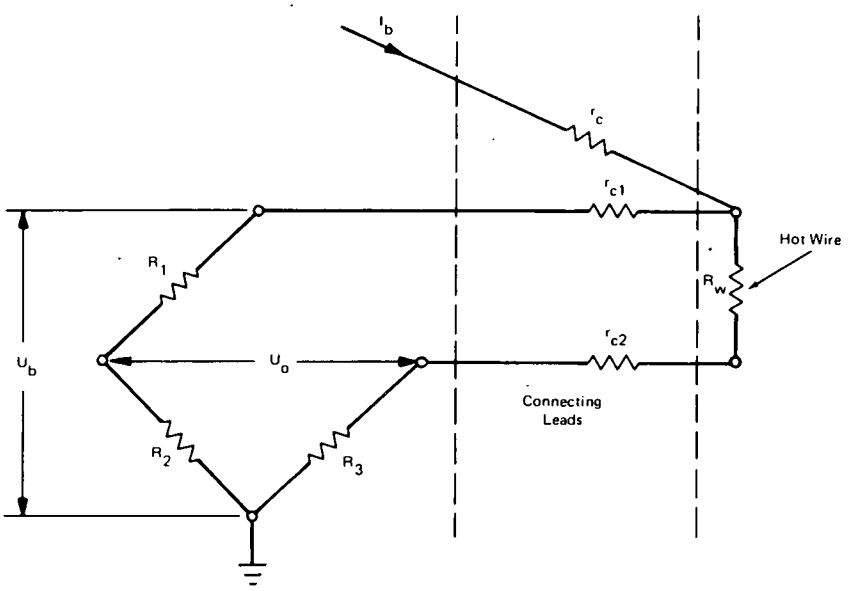
The cable-length constraint can be overcome by connecting the wire to the bridge with three leads. Two of these leads are placed in two legs of the bridge itself. The third lead, through which the bridge current I_b is fed, is not included in the bridge. A schematic of this three-lead terminal-wire bridge configuration is shown in the figure. The symbols, r_{c1} and r_{c2} denote the lead resistance of the two cables that are part of the Wheatstone bridge. The resistance of the cable through which the bridge-current flows is designated by r_c. The bridge-output voltage is U_b, and the unbalance voltage is denoted by U_o.

The bridge balance equation is

$$\frac{R_1+r_{c1}}{R_2} = \frac{R_w+R_{c2}}{R_3}, \tag{1}$$

where R_w designates the hot-wire (or sensor) resistance, R_2 and R_3 are two precision resistors of fixed value, and R_1 is the bridge rheostat balancing arm. Substitution of the bridge balance condition

$$R_w/R_3 = R_1/R_2, \tag{2}$$



Three-Lead Bridge Connection

into equation (1) leads to a ratio-arms relationship for the cable resistance in terms of either R_2 and R_3 or R_1 and Rw.

$$r_{c1}/r_{c2} = R_2/R_3 = R_1/R_w \quad (3)$$

Thus, the cable resistance is practically determined by the fixed resistors used in two arms of the bridge. When the lead resistance is properly selected to satisfy Equation (3), the bridge balance is completely unaffected by the cable resistance and, therefore, by their length. Such a bridge-terminal configuration permits the remote use of a hot-wire anemometer, which is of prime importance in atmospheric measurements and in many other experiments.

This new hot-wire terminal connection has been successfully used with cables up to 90 m (300 ft) long. The values of R_2 and R_3 and, therefore, the cable resistance, depends upon the wire resistance. If the maximum wire resistance is 10 Ω, then R_2/R_3 = 10; whereas if the former is 50 Ω then the latter is 2 Ω. In both cases R_1 = 100 Ω was used.

The frequency response of the hot-wire anemometer diminishes as the cable length increases. For instance, the frequency response of the CSU dual-amplifier hot-wire anemometer system reduces by about 30% (from 100 KHz to 70 KHz) when 90-m (300-ft) long cable is utilized.

Source: W. Z. Sadeh and C. L. Finn of
Colorado State University
under contract to
Marshall Space Flight Center
(MFS-21663)

Circle 17 on Reader Service Card.

TEMPERATURE COMPENSATION FOR VARACTOR DIODES

Frequency-multiplier circuits, employing varactor diodes as harmonic frequency-generating elements, are inherently temperature sensitive, due to the variation in diode properties with temperature. This temperature sensitivity is caused by the variation in depletion-layer capacitance and junction contact potential. Thermal energy imported to the free-charge carriers in the semiconductor material causes the contact potential to decrease, resulting in a narrowing of the depletion layer and thus increasing the junction capacitance.

Proper operation of a varactor diode requires the application of a dc bias voltage, by means of an external voltage source or by self-biasing with a shunt resistance. If the value of bias voltage changes, the associated change in diode capacitance will cause a detuning of the resonant portion of the circuit, producing an impedance mismatch. A reduction in power output may also result. The same detuning effect is encountered as the bias voltage changes, due to thermal variations.

A technique has been developed by which optimum bias resistance can be maintained as a function of temperature. The technique proposed is to have a correctly-tuned frequency-multiplier circuit operating at room temperature and to vary the ambient temperature while monitoring system performance. A graph of the shunt resistance required versus temperature then can be drawn.

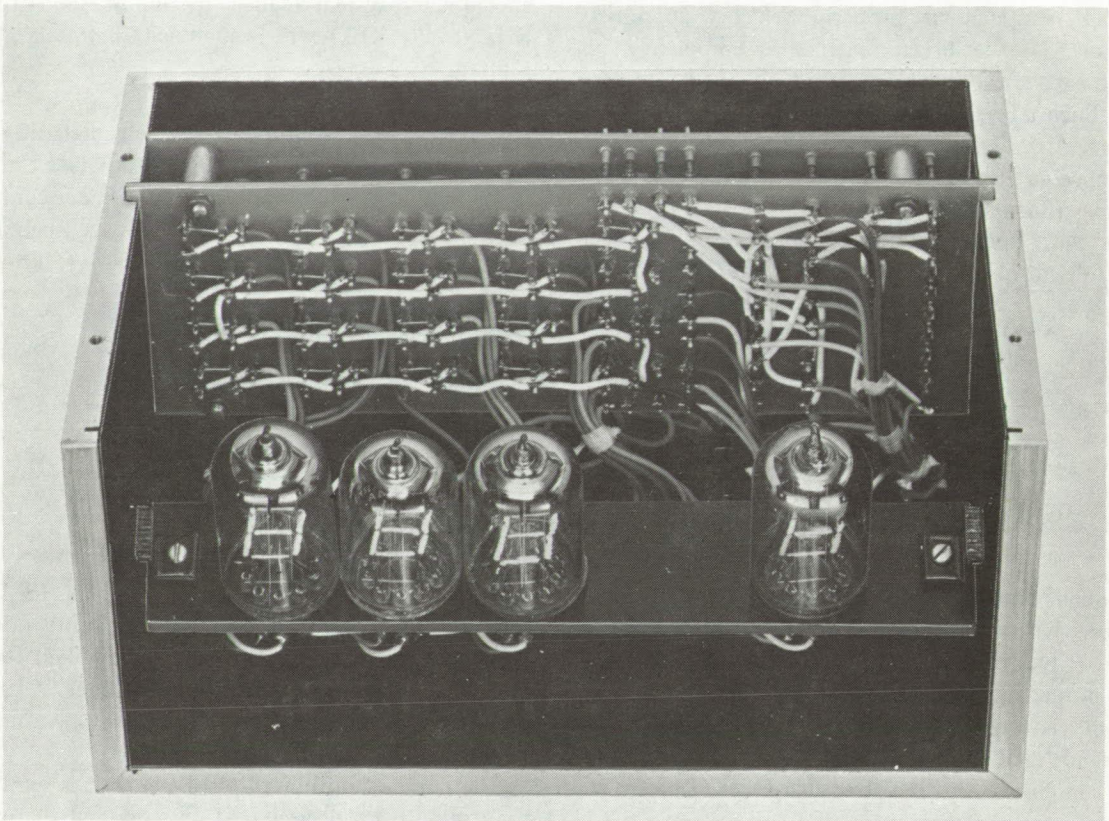
The curve of optimized resistance then is synthesized by a series-parallel circuit of resistors and thermistors. The network is connected across the varactor diode. The bias will remain optimized over a wide temperature range.

Source: J. D. Woermbke and
R. L. Zahn of
Westinghouse Electric Corp.
under contract to
Goddard Space Flight Center
(GSC-10045)

Circle 18 on Reader Service Card.

Section 3. Optical Equipment Circuits

LOW-VOLTAGE DIGITAL DISPLAY



Numerical Display Unit: Three-Quarter Front View,
Face Plate and Top Cover Removed

A numerical display unit (see figure) for computers has a wide, parallax-free viewing angle and may be seen from distances in excess of 40 ft (12.2 m).

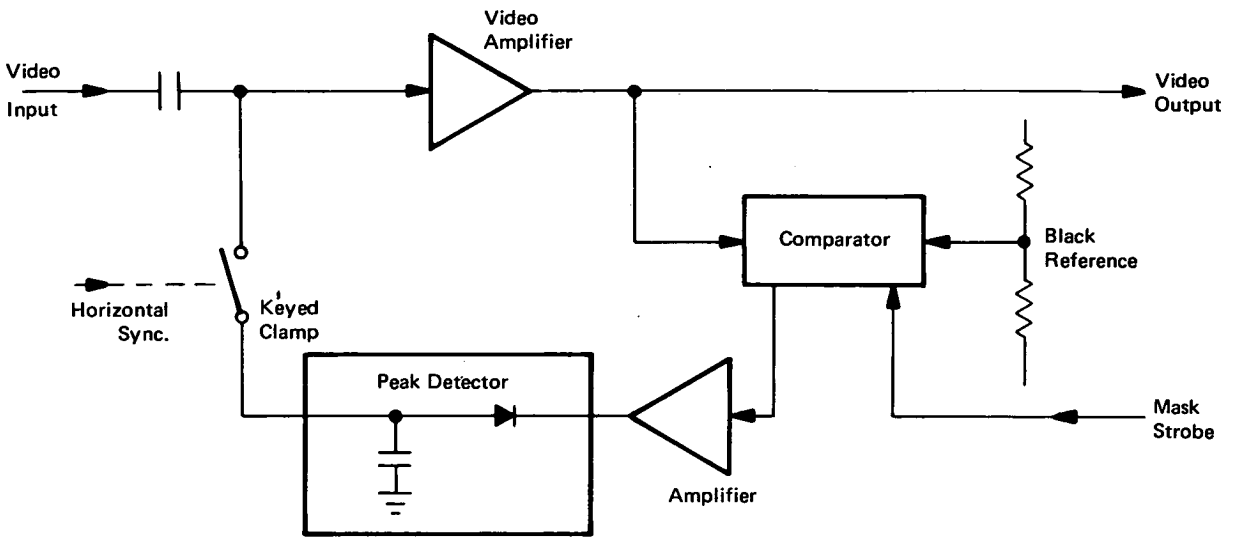
The display uses uniplanar seven-segment green fluorescent display tubes. The segments are controlled by logic gates and the 0- and 8-volt logic levels available at the computer-tape input. The number formation in the tubes makes the display readable from any angle. A tinted transparent faceplate covers the display, to prevent reflections.

The tubes can be switched reliably at less than 12 volts. (Typical operation for high brightness is 25 volts.) They are inexpensive, operate at the very high speeds of electronic control devices, and are limited only by the low persistence of the green phosphor.

Source: Jung P. Hong of
Caltech/JPL
under contract to
NASA Pasadena Office
(NPO-11334)

Circle 19 on Reader Service Card.

DARK-CURRENT COMPENSATION FOR SILICON TARGET-IMAGE TUBES



Block Diagram of Peak-Detector Process

A fundamental problem in the application of silicon target-image tubes is their relatively-large dark current. Dark current is present in all image tubes and is defined as that portion of the output signal which is independent of any light input. The dark current of a silicon target is a strong function of temperature. The problem has been dealt with in two ways.

In one method, a compensating signal is developed independently of the sensor. This method does not work well because the dark current of the existing tube increases as a function of time, so that error also increases.

In another method, a masked area of the image tube is used as a reference. This method also fails because unwanted and uncontrollable signals blemish the masked area, and saturated signals near the edge of the mask cause blooming.

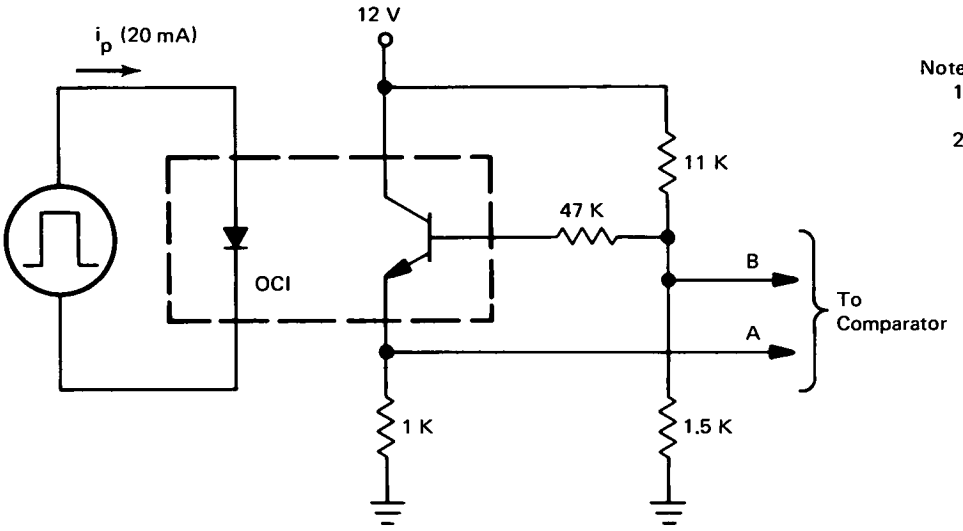
A successful solution to the problem also involves use of a masked area, but the level is read only during the horizontal retrace interval. In this way, a solid reference can be established without interference from extraneous signals on the target.

Instead of clamping at a fixed level, as in conventional systems, the clamping level is determined by sampling the video signal within the masked area. If this sampled signal is averaged over a complete vertical scan, then only line-to-line variation or streaking is avoided. Since any extraneous signals within the sampled area will be greater than the dark current, a peak-detection process can be used instead of averaging, to eliminate virtually all errors. A block diagram of the system is shown. A gated comparator compares the video to a fixed black reference level during the mask interval. The error signal is amplified and applied to a negative peak detector. It is assumed that the video at the sample point has a positive white polarity. The output of the peak detector then sets a reference for the keyed clamp. The video amplifier may be either inverting or noninverting so long as the polarity of the comparator is chosen to provide one net loop inversion. It must, however, be dc coupled.

Source: R. G. Popovich and
L. A. Thomas of
Westinghouse Electric Corp.
under contract to
Johnson Space Center
(MSC-14327)

Circle 20 on Reader Service Card.

LINEARLY BIASED OPTICALLY COUPLED ISOLATOR CIRCUIT



An optically coupled isolator (OCI) circuit has been linearly biased, allowing it to produce a larger output-voltage swing for a given rise and fall time. In comparison to conventional circuits, the OCI circuit provides tighter control over the output amplitude and improves the response speed by a factor of two or three. This circuit can be used to improve digital-pulse-transmission circuits that require dc isolation and high reverse-transmission rejection.

The linearly biased OCI circuit is shown in the figure. It consists of a light-emitting diode/phototransistor pair. The transistor, used as an emitter follower, operates only in its linear region. Resistors R_1 and R_2 provide the bias voltage. Bias is applied to the transistor through R_3 when the photodiode is in the off (dark) state. Due to the voltage drops across the base-emitter junction of the transistor and R_3, point B will be positive with respect to point A.

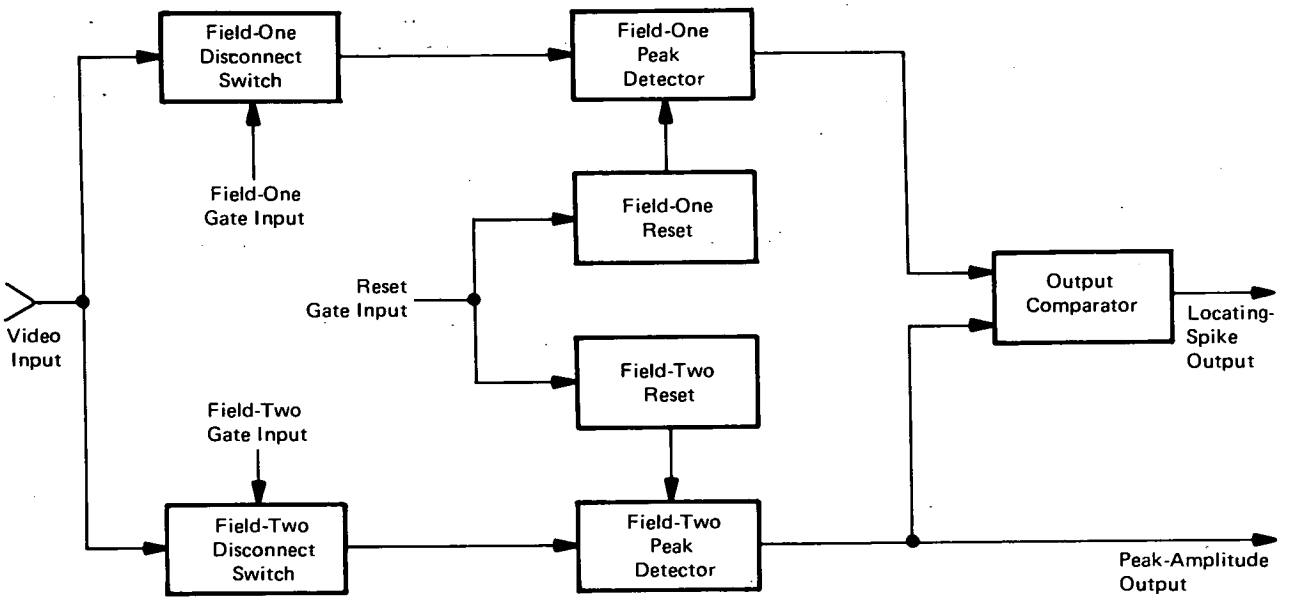
When the photodiode is in the on (luminous) state, photo-current induced into the transistor will exceed the bias current by a factor of three, causing point A to become positive with respect to point B and providing an input change to a comparator. In this state, R_3 permits the transistor base voltage to rise above the bias voltage, while permitting the coupler gain to remain essentially unchanged. Because emitter current flows in both states, the output impedance of the circuit does not change significantly from the off to the on state. Resistor R_3 acts effectively as a coupler-gain control, by bleeding off base current in direct proportion to the difference between the base voltage and the comparator reference-point (B) voltage. This keeps the amplitude relatively constant over a wide range of coupler gains.

Rise and fall times are minimized and controlled in the circuit, by maintaining sufficient junction currents to keep junction impedances low in relation to other circuit impedances. As a result, the output amplitude (which is a function primarily of the other circuit impedances) need not be sacrificed to obtain faster rise and fall times.

Source: I. McMeeking of
Martin Marietta Corp.
under contract to
Johnson Space Center
(MSC-14560)

Circle 21 on Reader Service Card.

VIDEO PEAK DETECTOR



A video peak detector has a low output impedance (200 ohms) and responds to a two-volt pulse, 120 nanoseconds wide (see figure).

The video signal is impressed on a detection comparator. The output is taken across a 390-picofarad capacitor through a very high-input impedance network comprised of two field-effect transistors (FET). The output is then fed back into the reference terminal of the comparator.

The comparator will only charge the capacitor when the signal voltage exceeds the reference voltage. The capacitor will then stay charged to more than 98 percent of the peak value over an entire frame.

Source: W. B. Boyer, J. Woods, and O. Graham
Johnson Space Center
(MSC-11605)

Circle 22 on Reader Service Card.

FAST RECHARGE CIRCUIT FOR Q-SWITCHED LASERS

Q-switched, cavity-dumped lasers employ an electro-optic-effect cell, such as a Pockels cell, to alternately block and release the laser pulse. The Pockels cell requires a high-speed switching circuit that can apply and remove a high voltage. The circuit must switch at rates greater than 5 kHz, should be solid-state to eliminate warmup time, should provide a variable voltage waveform, and should allow polarity reversal.

A new solid-state circuit employs complementary transistor switches and can meet all of these requirements. A simplified schematic of the circuit is shown in Figure 1. A high voltage is applied to the input terminal by a dc supply (not shown), and controlling commands are applied to the Q-Switching (QS) and

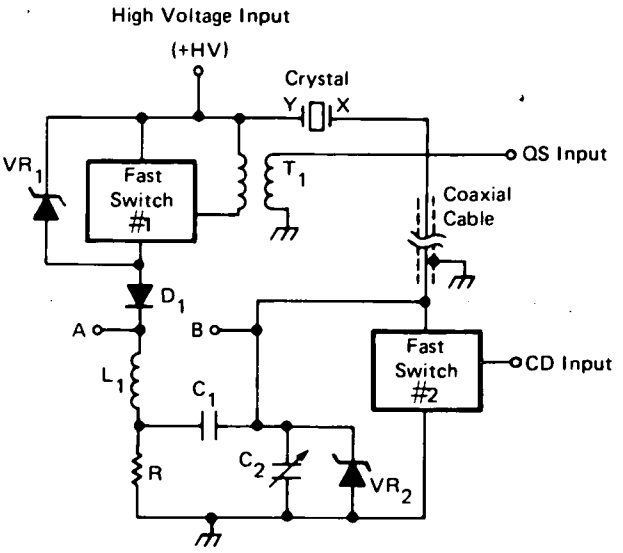


Figure 1. Switching Circuit

cavity-dumping (CD) terminals. The QS command is applied at a time t_0 (see Figure 2) to the primary of the high-voltage isolating transformer T_1. A triggering pulse is produced at the secondary T_1 and applied directly to fast switch #1 (a series-connected chain of 2N5401 pnp transistors). Before the signal is applied, the full high voltage is across the fast switch. Upon receipt of the QS command at t_0, the switch shorts, connecting the anode of diode D_1, and hence point A, rapidly to the high-voltage source. The rise time at point B (t_{rB}) may

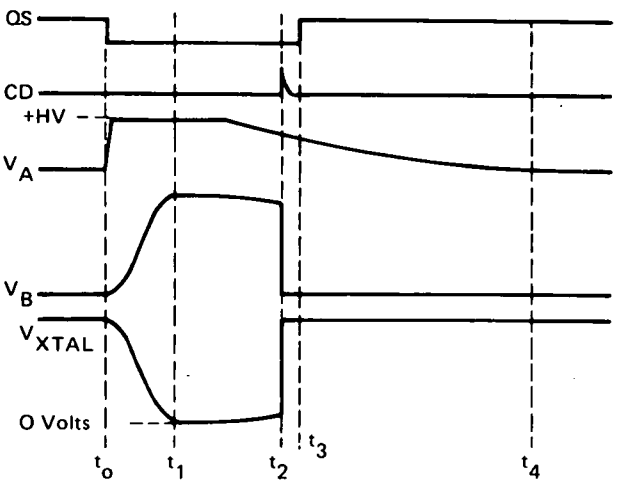


Figure 2. Timing Diagram

be determined from the following equation (if C_1 is $\gg C_B$).

$$t_{rB} = \sqrt{\pi (L)(C_B)},$$

where $C_B = C_2 + C_{CRYSTAL} + C_{VR2} + C_{FAST\ SWITCH\ \#2}$

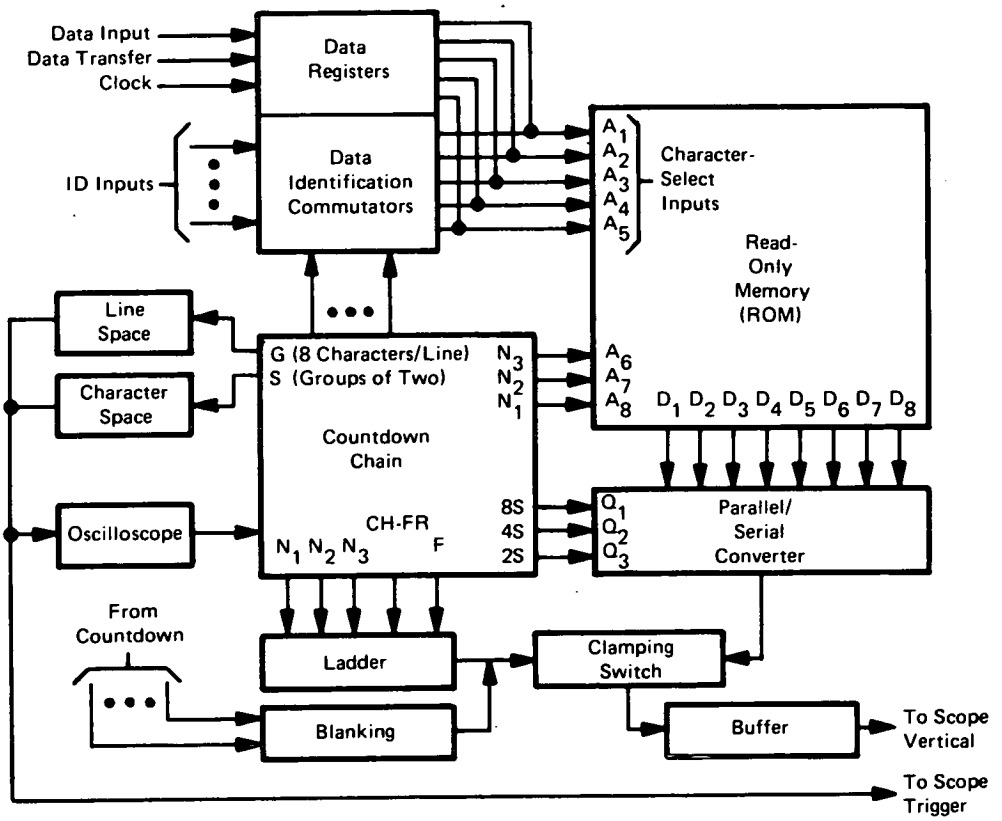
When the voltage level at B exceeds the voltage rating of zener diode VR2, further increase is clipped.

At some later time t_2, a pulse, applied at terminal CD by a pulse generator (not shown), causes fast switch #2 to short point B to ground. (Fast switch #2 is a series-connected chain of avalanche MPSU04 npn transistors.) This switching completes the generation of a high-voltage pulse suitable for the Pockels Cell. The polarity of the waveform applied to the Pockels Cell may be reversed simply by returning electrode Y to ground instead of the high-voltage source as shown. Another high-voltage pulse may be generated once the voltage at point A has returned to zero. Capacitor C1 isolates and protects fast switch #1 from #2 should a fault develop in either.

Source: R. L. Hansen of
GTE Sylvania Inc.
under contract to
Goddard Space Flight Center
(GSC-11510)

No further documentation is available.

ALPHANUMERIC CHARACTER GENERATOR FOR OSCILLOSCOPE



Block Diagram of Basic Character Generator

Printers and cathode-ray-tube (CRT) display terminals have been the most popular devices for presenting systems data. They are expensive, limited in application from model to model, and not truly portable.

A compact portable alphanumeric character-display device can be used with any general-purpose externally-triggered oscilloscope without need for Z-axis modulation.

The figure shows the character generator in block diagram. The generator pulses the oscilloscope external trigger, initiating a horizontal sweep of the scope trace. If no character segment is to be displayed, the vertical signal is inhibited by the clamping switch. When a segment is to be displayed, a pulse is generated in the desired position on the oscilloscope in the form of a short dash (segment). The vertical position of this segment is determined by the state of the ladder network. The alphanumeric characters are thus formed on the oscilloscope faceplate by the quantity and arrangement of these short dashes (segments). A read-only memory (ROM) contains the microprogram used to determine whether a segment is to be displayed or inhibited.

Factors that limit the size of the display are: output line capacitance, ROM speed, and persistence of the CRT. Capacitance must be kept to a minimum, because the output must switch very rapidly between the clamping voltage and the segment levels, in order to avoid annoying flicker.

Source: Donald C. Lokerson and
Ronald E. Boston
Goddard Space Flight Center
(GSC-11582)

Circle 23 on Reader Service Card.

VIDEO MULTIPLEXER/DEMULTIPLEXER SYSTEM

A high-speed, high-quality video multiplexing/demultiplexing system has been developed. The system employs pulse-amplitude modulation (PAM) techniques.

A PAM commutator sequentially samples three-color video signals, together with a synchronizing and calibrating signal, to form a composite waveform. The high sampling rate (2 MHz), together with signal quality requirements (linearity 1%, dynamic range 54 dB, bandwidth dc to 150 kHz), requires that an extremely good analog switching scheme be used.

A diode quadrature circuit has been designed for very fast switching. The commutating/decommutating phasing is such that the decommutating sample period occurs in the last half of the commutating period, in order to minimize crosstalk. The decommutating-sampling interval is only 250 ns.

The frequency spectrum of the PAM composite waveform contains dc components. Since previous circuits were ac coupled, special techniques were required. A method was devised to overcome this problem while still using the minimum number of PAM channels.

The performance of this equipment has met or exceeded design goals.

The following documentation may be obtained from:

American Institute of Aeronautics and Astronautics
750 Third Avenue
New York, N. Y. 10017

Reference: A68-37770, "Multiplexer/Demultiplexer Multi-Scan Cloud Camera for ATS-C"

Source: D. G. Kovar of
Hughes Aircraft Company
under contract to
Goddard Space Flight Center
(GSC-10578)

Patent Information

The following innovations, described in this Compilation, have been patented or are being considered for patent action as indicated below:

DC-to-AC-to-DC Converter (Page 7) GSC-11126

This invention has been patented by NASA (U.S. Patent No. 3,663,941). Inquiries concerning license for its commercial development may be addressed to:

Patent Counsel
Goddard Space Flight Center
Code 204
Greenbelt, Maryland 20771

Power Inverter With Sinusoidal Output (Page 9) MFS-21967

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457(f)], to: Martin Marietta Corporation, Denver, Colorado 80201.

Digital Servo Controller Behaves Like Synchro (Page 12) KSC-10769

and

Signal Conditioner Test Set (Page 16) KSC-10750

These inventions are owned by NASA, and patent applications have been filed. Inquiries concerning nonexclusive or exclusive license for their commercial development should be addressed to:

Patent Counsel
Kennedy Space Center
Code AD-PAT
Kennedy Space Center, Florida 32899

Variable-Frequency Inverter Controls Torque, Speed, and Braking in AC Induction Motors (Page 17) MFS-22088

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
Marshall Space Flight Center
Code AA01
Marshall Space Flight Center, Alabama 35812

Alphanumeric Character Generator for Oscilloscope (Page 25) GSC-11582

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for tis commercial development should be addressed to:

Patent Counsel
Goddard Space Flight Center
Code 204
Greenbelt, Maryland 20771

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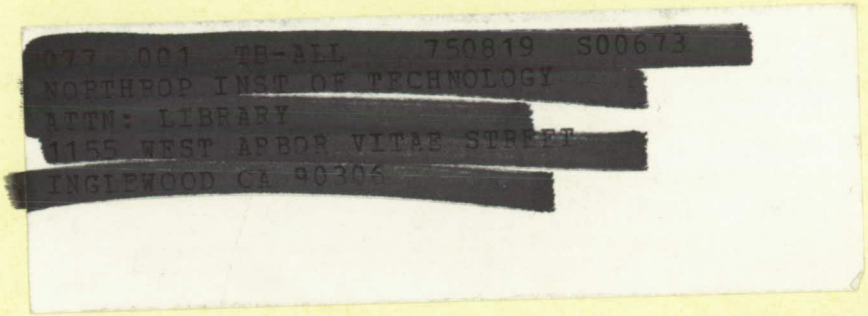

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